METHOD AND APPARATUS FOR DESIGN VERIFICATION WITH EQUIVALENCY CHECKING

ABSTRACT

Method and apparatus for design verification with equivalency checking is described. More particularly, an integrated circuit design for a device having programmable logic is obtained, and a test case design having one or more test patterns is obtained to test the integrated circuit design. Memory states for the test patterns are obtained and applied to configure at least a programmable logic portion of the integrated circuit design with at least one test pattern to provide a configured design. Equivalency checking with the at least one test pattern and the configured design may be done to determine if the configured design is functionally equivalent to the at least one test pattern.